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DESCRIPTION

REPRODUCTION SIGNAL PROCESSOR

Technical Field

The present invention relates to a reproduction signal processor and, more particularly, to a reproduction signal processor for converting an analog reproduction signal into a digital reproduction signal and performing automatic equalization.

Background Art

Conventionally, in a recording and reproduction apparatus, a communication apparatus or the like for digital information, an automatic equalizer for consecutively performing automatic equalization is employed in the way or at the end of a transmission line in order to compensate deterioration of signals by such as data errors due to characteristics of these apparatuses or the quality of the transmission line.

Figure 7 is a block diagram illustrating a structure of a conventional reproduction signal processor in the recording and reproduction apparatus for recording digital information.

The reproduction signal processor as shown in figure 7 is constituted by an analog/digital converter (A/D converter)

1, a digital phase locked loop (digital PLL) 2, and an automatic equalizer 9. The automatic equalizer 9 is further constituted by a transversal filter 4 and a control unit 5.

The analog/digital converter 1 samples an analog reproduction signal which is input to the reproduction signal processor into the digital reproduction signal with a large number of values. The digital phase locked loop 2 generates a reference clock CK which coincides with the phase included in the digital reproduction signal and the reference frequency component. The transversal filter 4 performs waveform equalization of the digital reproduction signal. The control unit 5 controls a tap coefficient as a parameter of the transversal filter 4 by using an equalization error which is an error between the equalized waveform output from the transversal filter 4 and an equalization target value estimated from the equalized waveform, and the digital reproduction signal which is input to the transversal filter 4, such that the equalization error becomes minimum.

Next, an operation of the conventional reproduction signal processor will be described with reference to figure 7.

a1 ~~The digital information which is recorded on a recording medium is read by a scan of a head not shown, and the read signal is subjected to a processing for emphasizing a predetermined frequency band to result in an analog reproduction signal, which is input to the analog/digital converter 1 to be converted to~~

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~~a multi-value digital reproduction~~ signal. Then, ~~the digital~~ reproduction signal is input to both of the digital phase locked loop 2 and the transversal filter 4 of the automatic equalizer 9. The digital phase locked loop 2 extracts the reference clock CK by the input digital reproduction signal, and inputs the reference clock CK to the analog/digital converter 1 and the automatic equalizer 9. The reference clock CK is used as an operation clock in the analog/digital converter 1 and the automatic equalizer 9. On the other hand, the digital reproduction signal input to the transversal filter 4 is transmitted to a decoding circuit after the equalization in the transversal filter 4. In the equalization, the transversal filter 4 is controlled by the tap coefficient as its parameter. The tap coefficient is set from the input digital reproduction signal to the transversal filter 4 and an equalization error which is an error between an output signal from the transversal filter 4 and an equalization target value estimated on the basis of the output signal, in the control unit 5 at appropriate timings. Typically, in the control unit 5, an LMS algorithm for consecutively performing operations on the basis of a steepest descent method so that the square mean of equalization target values ~~becomes the minimum, is used.~~

Here, a setting method of the equalization target value will be described. The equalization target value is one for setting the frequency characteristics of the equalizer (FIR

filter) when performing digital equalization. Usually, the equalization target value is set in consideration of the frequency characteristics of the signal to be input.

Figure 8(a) is a diagram illustrating an example of a digital reproduction waveform in the case of performing sampling by using the reference clock included in the digital reproduction waveform as the operation clock of the analog/digital converter 1.

The sequence of the numeral 1 or 0 which is shown at the upper part of the waveform shown in figure 8(a) is an example of codes recorded on the recording medium. The sampling points under the recorded codes are the sampling points corresponding to the recorded codes, respectively. In this stage, there is only provided an insufficient equalization, and therefore, it is in a situation where the amplitude of the reproduction waveform corresponding to short codes is hard to be output. In order to obtain the equalization target value on the basis of the waveform shown in figure 8(a), processings are performed in the following procedures.

Initially, in order to easily identify whether the sampling point is on the positive side or on the negative side with reference to zero, data which is input to the control unit 5 and data which is input one sampling before are added (1+D processing). The sampling data after being subjected to this process is shown in figure 8(b). An example of positive and

negative judgment result when the judgment is performed such that positive value and negative value are 1 and 0, respectively, is shown at the upper part of the waveform in figure 8(b). Practically, the judgment of positive or negative is performed by seeing the most significant bit of the waveform data after being subjected to 1+D processing. What should be noted here is that the recorded codes shown in figure 8(a) coincide with the array of data of "1" or "0" as the positive and negative judgment result shown in figure 8(b). In this way, when the recorded codes and the positive and negative judgment result coincide with each other, it is possible to securely set the equalization target value. It is because, when the recorded codes coincide with the positive and negative judgment result, it is possible to previously know a waveform of which length period should come next by tracing the data sequence of 1 and 0 sequentially.

Next, how the equalization target value is actually assigned will be described. When judgment results of positive or negative are added for every four samplings, the result of the addition becomes either of five values, 0, 1, 2, 3, or 4, and each value is assigned corresponding to one equalization target value. Figure 8(c) is a diagram showing this state. As shown in figure 8(c), 0 to 4 as the addition results of positive or negative correspond to levels A to E. 0, 1, 2, 3 and 4 correspond to level E, level D, level C, level B and level A,

respectively. By performing the above-described process, the equalization target value can be exactly set. However, what should be noted here is that the judgment results of positive or negative have to coincide with the recorded codes as a precondition for the setting of the equalization target value by this process. That is, it is essential that the reference clock included in the reproduction signal is employed as the operation clock of the analog/digital converter 1 so as not to occur omission of sampling of data. As long as this condition is kept, even when an asymmetry is generated due to the influences by noises or the pit formation of the disc, the setting of the equalization target value, which can entirely ignore these influences, is possible.

As described above, in the conventional reproduction signal processor, the signal deterioration can be compensated by consecutively performing waveform equalization using the reference clock extracted by the digital phase locked loop 2.

On the other hand, in Japanese Published Patent Application No. Sho.62-2724, a setting method of a filter coefficient vector for a transversal filter in a waveform equalization apparatus using an adaptive transversal filter is disclosed. In addition, in Japanese Published Patent Application No. Hei.3-100971, an automatic equalizer which can automatically control the characteristics parameter is also disclosed.

However, in the conventional reproduction signal processor as described above, the reference clock CK of the digital reproduction signal extracted by the digital phase locked loop 2 is supplied to the analog/digital converter 1 and the automatic equalizer 9 as the operation clock, thereby to reproduce the digital data. Therefore, while the digital data is being reproduced, the analog/digital converter 1 and the automatic equalizer 9 always keep operating. That is, the transversal filter 4 as a component of the automatic equalizer 9 and also the control unit 5 which controls the parameters of the transversal filter 4 always keep consuming power. Further, the rate of the automatic equalizer 9 occupying in the reproduction signal processor amounts to a little over 20 percent, whereby the consumption power thereof cannot be ignored.

In recent years, in the digital data reproduction apparatus, the speed-up of the data transfer speed is advancing, and the high-speed reproduction has become essential. The increase in the reproduction speed leads to an increase in the frequency of the reference clock included in the digital reproduction signal. This also leads to an increase in the frequency of the operation clock in the analog/digital converter 1 and the automatic equalizer 9. In this way, the high-speed reproduction is directly tied in with the increase in the power consumption. Further, in order to perform

high-speed reproduction with stability, it is necessary that the precision of signal processing and a time sufficient for positively performing signal processing are ensured, and the increase in the circuit scale due to an insertion of a delay element which is involved for keeping the number of the arithmetic bits and for keeping the number of bits cannot be avoided. Increasing the circuit scale leads to an increase in the power consumption.

A large amount of power consumption means that the temperature of the chip easily rises when the chip is integrated into an LSI or the like. When the LSI is built of mixed analog-digital chips, the increasing chip temperature makes it difficult for the characteristics of an analog element or the like to meet its specifications. That is, in order to sufficiently derive total performance as the chip, a low power consumption of not only the automatic equalizer 9 but also the whole LSI is desired.

Then, it is considered that the frequency of the operation clock which is supplied to the automatic equalizer 9 and the analog/digital converter 1 is lowered as a measure for realizing the reduction in power consumption and the correspondence to the high-speed reproduction. For example, a case is assumed that a 2-frequency-divided clock which has a period twice as that of the reference clock CK of the digital reproduction signal extracted by the digital phase locked loop 2 is the

operation clock of the automatic equalizer 9 and the analog/digital converter 1. When the operation clock is 2-frequency-divided, the power consumption can be reduced approximately by half. In addition, when the frequency-divided clock is supplied to the analog/digital converter 1 and is operated, the sampling number is reduced to half the number when the reference clock CK is supplied.

However, in the prior art, the omission of this sampling number prevents the automatic equalizer 9 from operating with stability, because the equalization target value is generated by utilizing the data continuity when the analog/digital converter 1 is sampled by the reference clock included in the digital reproduction signal, as described in the setting method of the equalization target value. There has been a problem that the sampling number is reduced to half, thereby ruining the data continuity and making the stable and faithful setting of the equalization target value difficult, and therefore, the stable equalization cannot be performed.

The present invention is made to solve these problems, and has its object to provide a reproduction signal processor which reduces the power consumption and has the automatic equalizer corresponding also to the high-speed reproduction, without lowering the equalization performance.

Disclosure of the Invention

In a reproduction signal processor of Claim 1 of the present invention comprising: an analog/digital converter for sampling an analog signal, and converting the same into the digital signal; an automatic equalizer for performing an automatic equalization of the digital signal; a phase locked loop for generating a reference clock which coincides with a phase included in the digital signal and reference frequency components; and a frequency divider for generating a frequency-divided clock obtained by performing integral multiplication of the period of the reference clock, and outputting the frequency-divided clock as an operation clock to the analog/digital converter and the automatic equalizer, the automatic equalizer is composed of: a transversal filter for performing waveform equalization of the digital signal; a straight-line interpolation unit for interpolating the omission of the sampling number due to sampling using the frequency-divided clock in the output of the transversal filter; and a control unit for estimating an equalization target value in accordance with the output of the transversal filter, and controlling a parameter of the transversal filter such that an equalization error which is an error between the equalization target value and the output of the transversal filter becomes minimum.

According to the present invention, the omission of the sampling points due to using the frequency-divided clock in

place of the reference clock can be compensated, and while keeping similar equalization performance as in the case of using the reference clock, the reduction in the power consumption and the correspondence to the high-speed reproduction can be realized.

According to a reproduction signal processor of Claim 2 of the present invention, in the reproduction signal processor of Claim 1, the straight-line interpolation unit is composed of: a flip-flop element for performing delay processing of an output equalization signal of the transversal filter for one period of the frequency-divided clock; and an adder for adding a signal after the delay processing and the output equalization signal.

According to the present invention, the omission of the sampling points due to using the frequency-divided clock in place of the reference clock can be compensated, and while keeping similar equalization performance as in the case of using the reference clock, the reduction in the power consumption and the correspondence to the high-speed reproduction can be realized.

According to a reproduction signal processor of Claim 3 of the present invention, in the reproduction signal processor of Claim 1, instead of the straight-line interpolation unit, a high-order interpolation unit for interpolating the omission of the sampling number due to sampling using the frequency-

divided clock in the output of the transversal filter is provided.

According to the present invention, the omission of the sampling points due to using the frequency-divided clock in place of the reference clock can be compensated, and while keeping similar equalization performance as in the case of using the reference clock, the reduction in the power consumption and the correspondence to the high-speed reproduction can be realized. Further, an information restoring capacity for the quality deterioration of the reproduction waveform data because of a damping of an amplitude due to characteristics deterioration of a reading head, waveform distortion caused by a tilt of a disc, and influences of noises which are superimposed in a reproduction system, can be improved.

According to a reproduction signal processor of Claim 4 of the present invention, in the reproduction signal processor of Claim 3, the high-order interpolation unit is composed of: a flip-flop element for performing delay processing for one period of the frequency-divided clock; plural multipliers for performing weighting of a tap coefficient on a signal after the delay processing; and an adder for adding an output signal of the plural multipliers.

According to the present invention, the omission of the sampling points due to using the frequency-divided clock in place of the reference clock can be compensated, and while

keeping similar equalization performance as in the case of using the reference clock, the reduction in the power consumption and the correspondence to the high-speed reproduction can be realized. Further, an information restoring capacity for the quality deterioration of the reproduction waveform data because of a damping of an amplitude due to characteristics deterioration of a reading head, waveform distortion caused by a tilt of a disc, and influences of noises which are superimposed in a reproduction system, can be improved.

Brief Description of the Drawings

Figure 1 is a block diagram illustrating a structure of a reproduction signal processor according to a first embodiment of the present invention.

Figure 2(a) is a diagram showing an example of an input digital reproduction signal of an automatic equalizer using a frequency-divided clock according to the first embodiment of the present invention.

Figure 2(b) is a diagram showing an example of an output equalized waveform of the automatic equalizer using a frequency-divided clock according to the first embodiment of the present invention.

Figure 2(c) is a diagram showing an example of an output equalized waveform of the automatic equalizer using a reference clock.

Figure 3(a) is a diagram showing an example of the output equalized waveform of the automatic equalizer using the frequency-divided clock according to the first embodiment of the present invention.

Figure 3(b) is a diagram showing an example of the result after being subjected to 1+D processing according to the first embodiment of the present invention.

Figure 3(c) is a diagram showing an example of an interpolated waveform which is restored by using waveform data subjected to timing adjustment according to the first embodiment of the present invention.

Figure 4 is a block diagram illustrating a structure of the reproduction signal processor according to a second embodiment of the present invention.

Figure 5 is a diagram illustrating an example of a high-order interpolation unit according to the second embodiment of the present invention.

Figure 6 is a diagram showing an example of a Nyquist interpolation as an example of the high-order interpolation according to the second embodiment of the present invention.

Figure 7 is a block diagram illustrating a structure of a conventional reproduction signal processor.

Figure 8(a) is a diagram showing an example of the output waveform of an analog/digital converter in the conventional reproduction signal processor.

Figure 8(b) is a diagram showing an example of the result after subjecting the output waveform of the analog/digital converter to 1+D processing in the conventional reproduction signal processor.

Figure 8(c) is a diagram showing an example of the output waveform of the result after setting an equalization target value in the conventional reproduction signal processor and performing equalization.

Best Mode for Carrying out the Invention

(Embodiment 1)

Hereinafter, a reproduction signal processor according to the first embodiment of the present invention will be described with reference to the drawings.

Figure 1 is a block diagram illustrating a structure of the reproduction signal processor according to the first embodiment of the present invention.

The reproduction signal processor shown in figure 1 is constituted by an analog/digital converter 1, a digital phase locked loop 2, a frequency divider 3, and an automatic equalizer 8. The automatic equalizer 8 is further constituted by a transversal filter 4, a control unit 5, and a straight-line interpolation unit 6. Further, the same numerals as in figure 7 show the same objects as in the conventional reproduction signal processor, and the explanation thereof is omitted.

The frequency divider 3 subjects the reference clock CK extracted by the digital phase locked loop 2 to frequency dividing process for performing integral multiplication of the period of the reference clock CK. The straight-line interpolation unit 6 is composed of a flip-flop element not shown and an adder. In the sampling in the analog/digital converter 1, the interpolation is performed for compensating the omission of the sampling number due to using the frequency-divided clock CK/N in place of the reference clock CK.

Next, the operation of the reproduction signal processor will be described with reference to figure 1.

~~The digital information which is recorded on a recording~~ medium is read by a scan of a head not shown, and the read signal is subjected to a processing for emphasizing a predetermined frequency band to result in an analog reproduction signal, which is input to the analog/digital converter 1 to be converted to a multi-value digital reproduction signal. Then, the digital reproduction signal is input to both of the digital phase locked loop 2 and the transversal filter 4 of the automatic equalizer 8. The digital phase locked loop 2 extracts the reference clock CK by the input digital reproduction signal, and inputs the reference clock CK to the frequency divider 3. The frequency divider 3 performs frequency dividing process for performing ~~integral multiplication of the period of the reference clock~~

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~~CK~~, and outputs a ~~frequency-divided clock CK/N~~. The frequency-divided clock CK/N is used as the operation clock in the analog/digital converter 1 and the automatic equalizer 8. Here, N denotes the division ratio, and the frequency-division ratio is referred to as N=2 in this first embodiment (hereinafter, referred to as "2-frequency-division"). On the other hand, the digital reproduction signal input to the transversal filter 4 is transmitted to a decoding circuit after the equalization in the transversal filter 4. In the equalization, the transversal filter 4 is controlled by the tap coefficient as the parameter. The tap coefficient is set from the digital reproduction signal input through the transversal filter 4, and an equalization error which is an error between an output signal from the transversal filter 4 and an equalization target value, in the control unit 5 at approximate timings. Typically, in the control unit 5, an LMS algorithm for consecutively performing operations on the basis of a steepest descent method so that the square mean of equalization target values becomes the minimum, is used. As for the equalized waveform output from the transversal filter 4, by using the frequency-divided clock CK/N as the operation clock, the sampling number gets less than that in the case of using the reference clock CK. Thereby, in order to prevent the setting of the equalization target value in the control unit 5 from becoming unstable~~, the output~~ equalized waveform of the

~~transversal filter 4 is input to the control unit 5, and as well as the straight-line interpolation unit 6 performs interpolation in the output equalized waveform, the signal obtained by interpolating the samples which are omitted due to using the frequency-divided clock CK/N is also input to the control unit 5. Thereby, the setting of the equalization target value can be performed with stability, similarly as in the case of using the reference clock CK.~~

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Next, a straight-line interpolation will be described with reference to waveform charts, figures 2(a)-2(c) and figures 3(a)-3(c).

Figures 2(a)-2(c) and figures 3(a)-3(c) show an example of the digital reproduction signal, the equalized waveform, and the waveform obtained by performing the straight-line interpolation in the equalized waveform.

Figure 2(a) is a diagram showing an example of the digital reproduction signal, and ◇ shows the point obtained by sampling the analog reproduction signal by using the 2-frequency-divided clock (hereinafter, referred to as "a sampling point"). Figure 2(b) is a diagram showing the equalized waveform obtained by equalizing the digital reproduction signal in figure 2(a) by the transversal filter 4, and ◇ shows the sampling point after the waveform equalization. Figure 2(c) is a diagram showing the equalized waveform (an ideal waveform) in the case of using the reference clock, and ◇ shows the sampling point in the case

of using the reference clock as the operation clock, in the analog/digital converter 1. Further, solid lines which join the sampling points in figures 2(a)-2(c) are added so as to easily recognize the waveform.

According to the comparison between figure 2(b) and figure 2(c), when the 2-frequency-divided clock is used in place of the reference clock, it is known that the sampling number of the digital reproduction signal output by the analog/digital converter 1 decreases in accordance with the increase in the frequency division ratio. It is the straight-line interpolation performed by the straight-line interpolation unit 6 that the omission of the sampling number due to using the frequency-divided clock as described above is compensated.

Figures 3(a)-3(c) are diagrams showing examples of the straight-line interpolation to the equalized waveform which is sampled by using the 2-frequency-divided clock and is equalized. In figure 3(a), ● shows a point obtained by sampling the digital reproduction signal by the 2-frequency-divided clock in the analog/digital converter 1, and ○ shows a point to be sampled when the reference clock is used. That is, when the reference clock is assumed as the operation clock of the analog/digital converter 1, both of ● and ○ are sampled. Further, ● and ○ may be reversed by the timing that the sampling starts. Here, it is an interpolation process that ○ is falsely restored by using only ●. Initially, in figure 3(b), the result of

performing 1+D processing to ● in figure 3(a) is shown by ◇. Here, 1+D processing is a processing where one equalized sampling point is subjected to delay processing for one period of the operation clock by the flip-flop element, and the equalized sampling point is added thereto by the adder. To be specific, this processing is the operation of adding a difference of one sampling point from a sampling point as a reference (in figure 3, the leftmost sampling point is the reference) to the next sampling point, i.e., the sampling point which is delayed by one period of the 2-frequency-divided clock. The waveform in figure 3(c) is obtained by performing timing adjustment of ● shown in figure 3(a) and ◇ shown in figure 3(c), and this is the waveform after interpolation. Further, in order to easily recognize the waveforms, it is added that the sampling points are joined by the solid line or broken line in figures 3(a)-3(c).

Next, the setting method of the equalization target value in the case of using the frequency-divided clock will be described with reference to figure 3(c). This processing is performed in the control unit 5.

In figure 3(c), ● shows the data which is actually sampled by the frequency-divided clock, and ◇ is the result obtained by the straight-line interpolation, i.e., the 1+D processing that the output signal from the transversal filter 4 input to the present control unit 5 and the output of the transversal

filter 4 of one sampling in advance are added. Figure 3(c) showing the sampling data after this interpolation is subjected to the 1+D processing, and, as for the result of the 1+D processing for three successive pieces of ● and two successive pieces of ◇, whether each sampling is positive or negative is determined, thereby performing the processing corresponding to figure 8(b). However, the addition result utilizes only the most significant bit of the adder. Similarly as described in the prior art, five levels, 0 to 4 are provided by adding only the most significant bits in these output results of the adder. Therefore, the equalization target value can be set similarly as in the case of using the reference clock.

As described above, in the reproduction signal processor according to the first embodiment of the present invention, the operation clock used in the analog/digital converter 1 and the automatic equalizer 8 constitutes the frequency-divided clock, thereby reducing the power consumption. Furthermore, long processing intervals in each component part can be taken as compared with when the reference clock is used. Therefore, the reproduction signal processor can correspond also to the high-speed reproduction and suppress an increase in the circuit scale.

In addition, the automatic equalizer 8 comprises the straight-line interpolation unit 6, thereby compensating the omission of the sampling points due to using the frequency-

divided clock in place of the reference clock, enabling the setting of the equalization target value in the control unit 5 to be performed with stability, and keeping an equalization capacity equal to that in the case of using the reference clock.

Further, in the reproduction signal processor according to the first embodiment of the present invention, the frequency-division ratio is referred to as N=2. However, this is an example, and for example, the frequency-division ratio may be referred to as N=3. However, it is within the range where the interpolation can be performed by the interpolation to the similar degree as when the sampling is performed by the reference clock that the frequency-division ratio can be increased. For example, when having such a frequency-division ratio that the period of the frequency-divided clock exceeds a minimum repetition period of the reproduction signal, the equalization cannot be performed with stability.

(Embodiment 2)

Hereinafter, the reproduction signal processor according to the second embodiment of the present invention will be described with reference to the drawings.

Figure 4 is a block diagram illustrating a structure of the reproduction signal processor according to the second embodiment of the present invention. Further, the same numerals are used concerning the same structure as that of the above-described first embodiment, and an explanation thereof

is omitted.

A high-order interpolation unit 7 shown in figure 4 performs a high-order interpolation such as the Nyquist interpolation or the like, in the sampling in the analog/digital converter 1, in order to compensate the sampling points which are omitted due to using the frequency-divided clock in place of the reference clock. The Nyquist interpolation is composed of a flip-flop element which performs delay processing for one period of the frequency-divided clock, plural multipliers which perform weighting of the Nyquist interpolation on a signal after the delay processing, and an adder which adds plural multiplier output signals. Further, the straight-line interpolation according to the first embodiment is a process for interpolating by using a straight line. On the other hand, the high-order interpolation according to the second embodiment is a process for interpolating by using a high-order curve such as the second-order or the higher-order.

Next, the operation of the reproduction signal processor will be described with reference to figure 4. Further, regarding the same operation as in the above-described first embodiment, an explanation thereof is omitted.

The high-order interpolation unit 7 has the similar role as that of the straight-line interpolation unit 6 described in the first embodiment, that is, the role of supplying the waveform, which appears as if there was no omission of

information, to the control unit 5, in the case where the sampling number is decreased by using the frequency-divided clock as the operation clock of the analog/digital converter 1 and the automatic equalizer 8. Figure 5 is a diagram illustrating an example of the high-order interpolation unit 7. The high-order interpolation unit 7 may be, for example, an FIR filter composed of delay elements 10a to 10f, multipliers 11a to 11g, and an adder 12. C1 to C7 represent weighting coefficients of the filter. The Nyquist interpolation is performed by selecting the Nyquist interpolation characteristics shown in figure 6 as these coefficients, thereby compensating the omission of the sampling number with using the frequency-divided clock as the operation clock. Here, an axis of ordinates in figure 6 shows the weighting coefficient. For example, when one point is made to be the weighting coefficient C1 of the filter, a point of being increased by 1T concerning an axis of abscissas from its point is made to be a weighting coefficient C2, and a point of being increased by further 1T is made to be a weighting coefficient C3, thereby determining the respective weighting coefficients C1 to C7. Further, the weighting coefficients of the filter is set by a register or the like, and the weight can be changed by the change of a register value. The high-order interpolation unit 7 as shown in figure 5 is employed, thereby sharply improving an information restoring capacity for the quality deterioration

of the reproduction waveform data such as a damping of an amplitude due to characteristics deterioration of a reading head, waveform distortion caused by a tilt of a disc, and influences of noises which are superimposed in a reproduction system, as compared with the case of using the straight-line interpolation unit 6.

As described above, the reproduction signal processor according to the second embodiment employs the high-order interpolation unit 7, and supplies the interpolated waveform obtained by interpolating the omission of information which is caused by using the frequency-divided clock to the control unit 5, thereby setting the stable and suitable equalization target value. Therefore, even in the case of using the frequency-divided clock, the equalization performance which is equal to that in the case of using the reference clock can be realized.

In addition, an information restoring capacity for the quality deterioration of the reproduction waveform data such as a damping of an amplitude due to characteristics deterioration of a reading head, waveform distortion caused by a tilt of a disc, and influences of noises which are superimposed in a reproduction system, can be improved by employing the high-order interpolation unit 7.

Industrial Availability

As described above, the reproduction signal processor

according to the present invention is the one for converting the analog reproduction signal into the digital reproduction signal and performing automatic equalization of the digital reproduction signal, and is suitable for automatic equalization of the reproduction signal which is reproduced at high speed or automatic equalization at low power consumption.